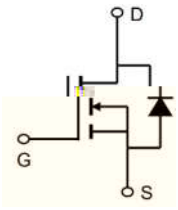
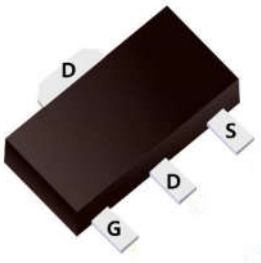
	30A
	60V
	30mΩ
	40mΩ





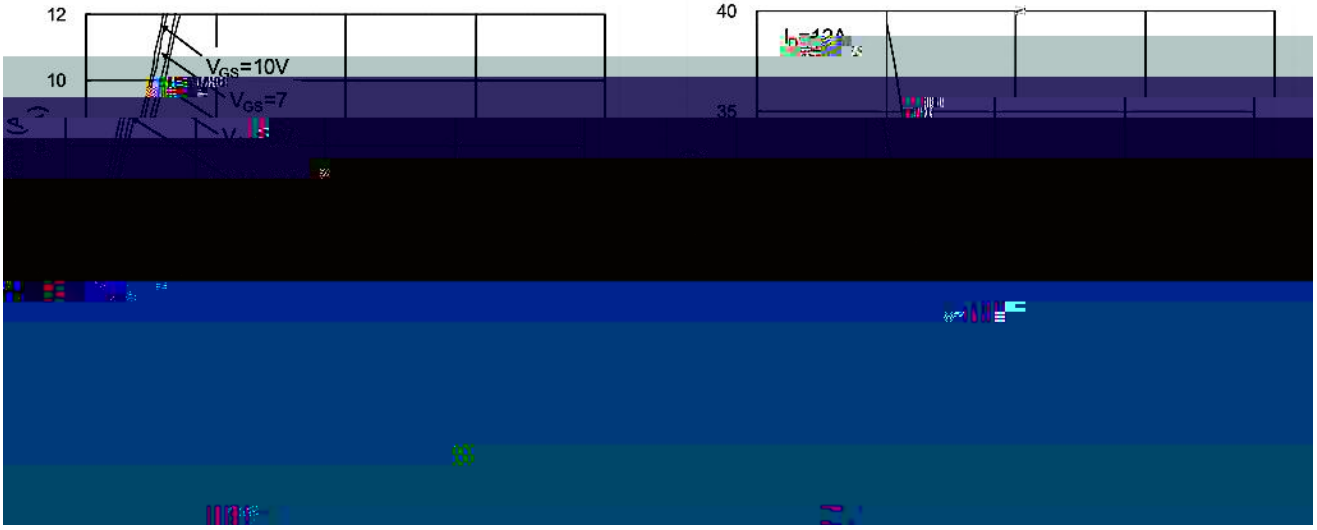
SOT-89

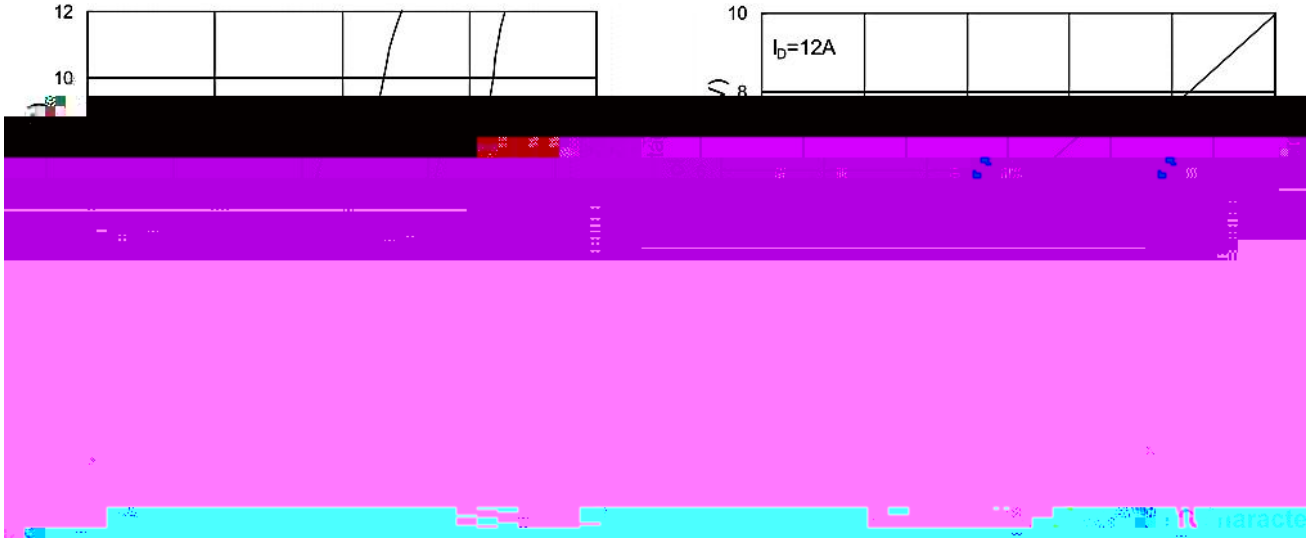
Marking Code	

- Lead free product is acquired
- High density cell design for ultra low RDS(on)
- Good stability and uniformity with high EAS
- Power Management
- Excellent package for good heat dissipation
- Power switching application
- Hard switching and high frequency circuits
- Uninterruptible power supply

Drain-Source Voltage			60	
Gate-Source Voltage			20	
Continuous Drain Current	TA=25		30	
	TA=100		18	
Pulsed Drain Current (Note 1)			114	
Single Pulse Avalanche Energy (Note 2)			25.5	
Power Dissipation			34.7	
Junction Temperature			-55-+150	
Storage Temperature			-55-+150	
Thermal Resistance From Junction to Ambient (note 3)			3.6	

Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA		60			
Drain-Source Leakage Current	V_{DS}=48V, V_{GS}=0V TJ=25				1	
	V_{DS}=48V, V_{GS}=0V TJ=55				5	
Gate-body Leakage	V_{DS}=±20V, V_{DS}=0V				±100	
Drain-Source On-Resistance (note 4)	V_{GS}=10V, I_D=15A			21	30	
	V_{GS}=4.5V, I_D=10A			28	40	
Gate-Threshold voltage	V_{DS}=VGS, I_D=250uA		1.2	1.6	2.5	
Diode forward voltage	I_S=1A, V_{GS}=0V				1.2	
Forward Transconductance	VDS=5V,ID=15A			17		
Gate Resistance	VDS=0V,VGS=0V,f=1MHz			3.2		
Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz			1378		
Output capacitance				86		
Reverse Transfer capacitance				64		
Total Gate Charge	V_{GS}=4.5V V_{DS}=48V I_D=12A			12.6		
Gate Source Charge				3.2		
Gate Drain(Miller) Charge				6.3		
Turn-on Time	V_{GS}=10V I_D=10A V_{DD}=30V R_{GEN}=3.3Ω			8		
Rise time				14.2		
Turn-off Time				24.4		
Fall time				4.6		
Continuous Source Current	VGS=VDS=OV,Force Current				23	
Pulsed Source Current					46	





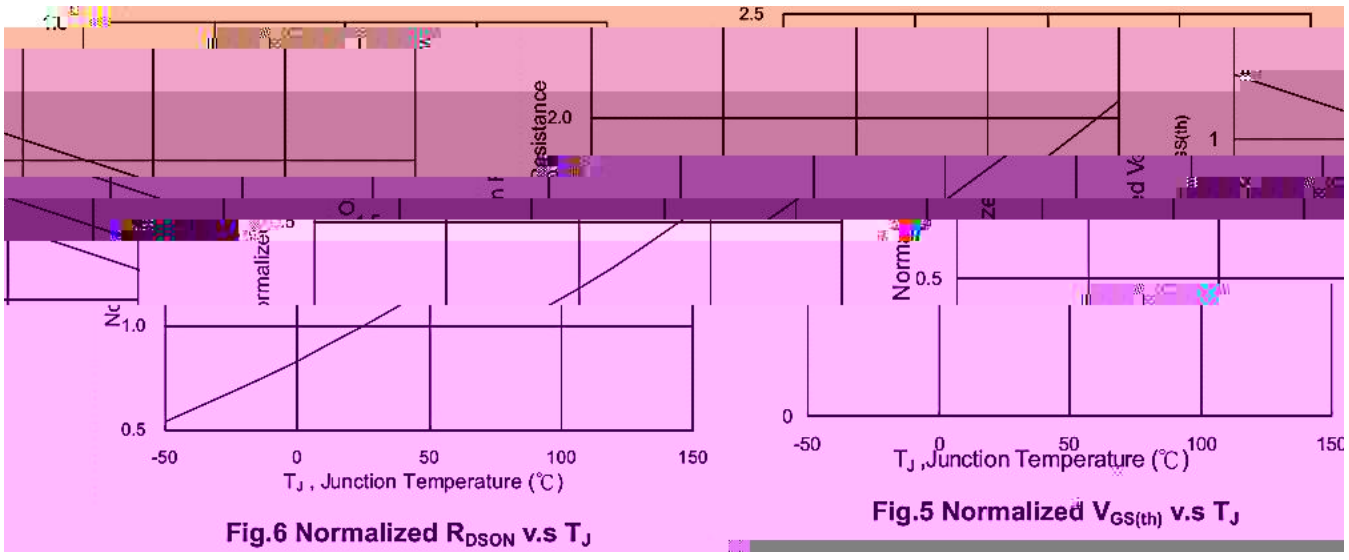
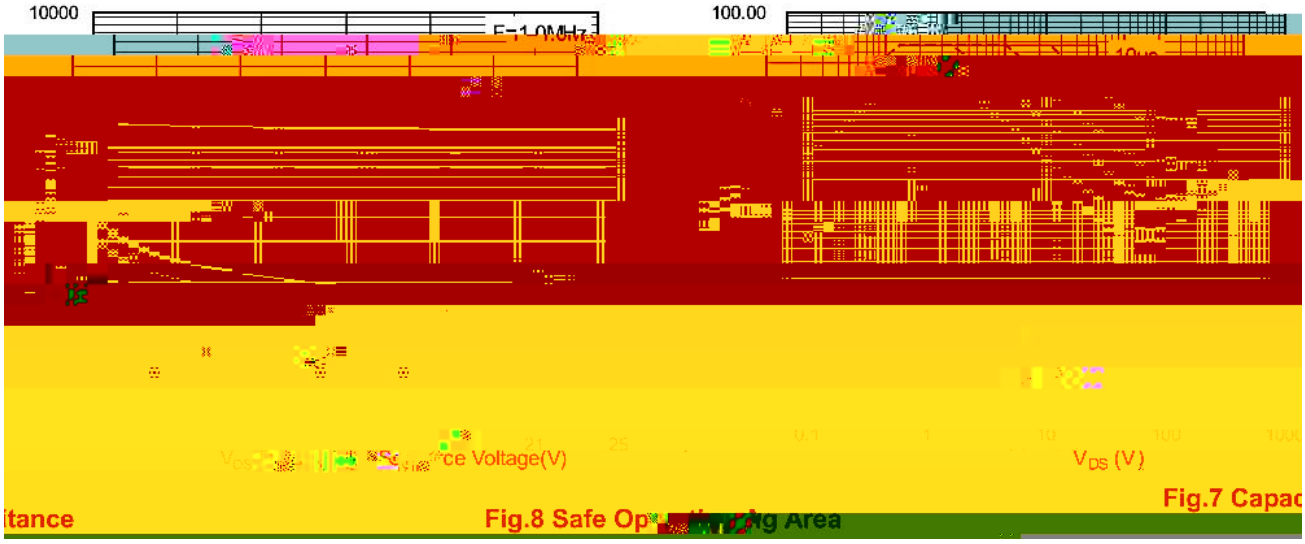
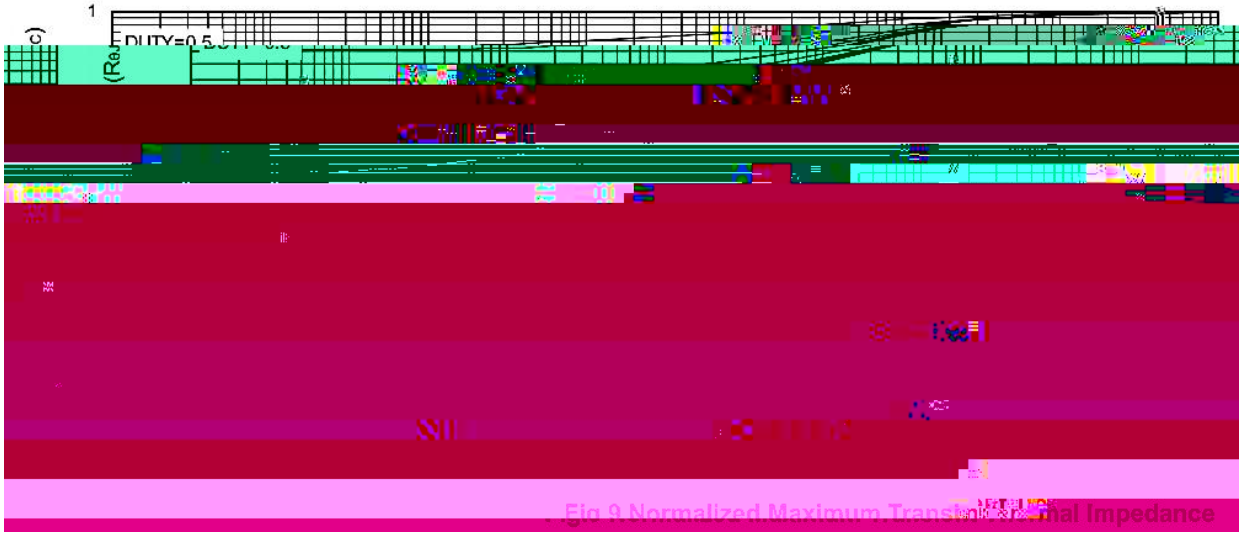
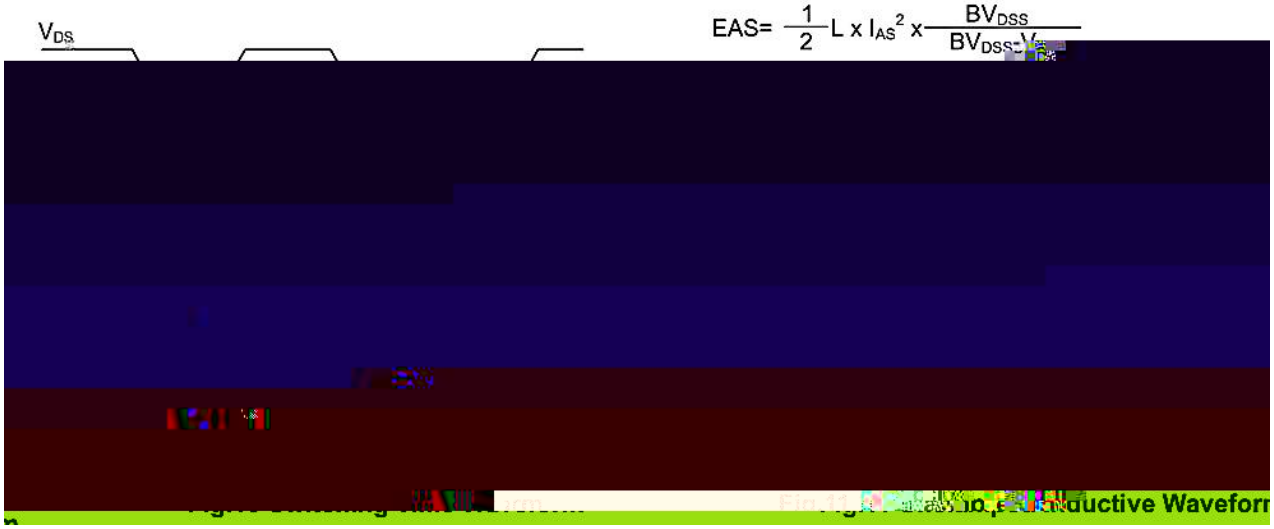


Fig.6 Normalized R_{DSON} v.s T_J

Fig.5 Normalized $V_{GS(th)}$ v.s T_J


10000
100.00
ce Voltage(V)
V_{DS} (V)
Fig.7 Capac
itance
Fig.8 Safe Op
g Area


1
Fig.9 Normalized Maximum Transi
mal Impedance


V_{DS}
$EAS= \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS}-V}$
ductive Waveforr

		””r1	0”

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